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| **National University of Computer and Emerging Sciences, Lahore Campus** | | | | |
| C:\Users\saif\AppData\Local\Microsoft\Windows\Temporary Internet Files\Content.Word\final design.jpg | **Course:** | **Digital Logic Design** | **Course Code:** | **EE-227** |
| **Program:** | **BS (Computer Science)** | **Semester:** | **Spring 2021** |
| **Duration:** | **15 Minutes** | **Total Marks:** | **10** |
| **Paper Date:** | **06/04/2022** | **Weight** |  |
| **Section:** | **2A** | **Page(s):** | **2** |
| **Exam:** | **Quiz 3** | **Roll No.** |  |
| **Instruction/Notes:** | **Calculators are strictly not allowed in all exams**  **Plagiarism will be dealt seriously causing an F in course** | | | |

**Question 01: [5 Marks]**

Design an 8–to–1-line multiplexer using a 3–to–8-line decoder and an 8X2 AND-OR.

**Question 02: [5M]**

Implement the Boolean function ***F*(*A*, *B*, *C*, *D*) = ∑*m*(1, 3, 4, 11, 12, 13, 14, 15)** with a 4–to–1-line multiplexer and external gates. Connect inputs *A* and *B* to the selection lines. The input requirements for the four data lines will be a function of the variables *C* and *D*. The values of these variables are obtained by expressing *F* as a function of *C* and *D* for each of the four cases when *AB* = 00, 01, 10 and 11. These functions must be implemented with external gates.